

IN THE SPECIFICATION:

On page 1, just before the title, please delete the present heading as follows:

~~Description~~

On page 1, immediately after the title, please insert the following paragraph and heading as follows:

This specification for the instant application should be granted the priority date of September 27, 2002, the filing date of the corresponding German patent application 102 46 083.3 as well as the priority date of September 25, 2003, the filing date of the corresponding International patent application PCT/DE2003/003264.

Background of the Invention.

On page 3, lines 4-6, please amend this paragraph as follows:

The invention ~~provided in claim 1~~ is based on the problem of producing a high voltage circuit which processes or makes available switching signal sequences at different voltage levels.

On page 3, line 7, please insert the following heading:

Summary of the Invention

On page 3, line 8, please delete this paragraph entirely as follows:

~~This problem is solved with the features set forth in claim 1.~~

On page 5, lines 23-24, please insert the following heading:

~~Advantageous embodiments of the invention are provided in claims 2 through 9.~~

On page 6, lines 2 -12, please amend this paragraph as follows:

According to ~~an~~ one embodiment of ~~claim 3~~, a third inverter circuit between the terminals Vdd and Vss allows the signal to be inverted twice from a low signal at the inlet IN, so that this is conducted in-phase to the input signal to the capacitor C1. The outlet of the third inverter circuit is connected with the inlet of the first inverter circuit of the voltage transmitter and its inlet is connected with the inlet of the second inverter circuit of the voltage transmitter as well as with the

terminal IN as the inlet of the circuit arrangement for bridging high voltage with a switching signal. The signal moves inverted via the second inverter circuit of the voltage transmitter to the capacitor C2. Thus, a differential operation is provided.

On page 6, line 14 through page 7, line 2, please amend this paragraph as follows:

A fourth and fifth inverter circuit between the terminals Vddh1 and Vddh2 are outlet inverters ~~as provided in claim 3~~, whereby the inlet of the fourth inverter circuit is connected with the inlet of the first inverter circuit of the voltage receiver, the inlet of the fifth inverter circuit is connected with the inlet of the second inverter circuit of the voltage receiver, the outlet of the fourth inverter circuit is connected with the terminal OUT1 as the first outlet of the voltage receiver and the outlet of the fifth inverter circuit is connected with the terminal OUT2 as the second outlet of the voltage receiver, ~~according to the embodiment of claim 3~~. Beginning as a low signal at the inlet of the voltage transmitter, on the outlet OUT1, a low signal with reference to the high-voltage voltage supply exists and on the outlet OUT2, a high signal with reference to the high-voltage voltage supply exists.

On page 7, lines 4-13, please amend this paragraph as follows:

A sixth and a seventh inverter circuit between the terminals Vdd and Vss according to ~~the~~ a further embodiment ~~of claim 4~~ are driver stages, whereby the inlet of the seventh inverter circuit is connected with the inlet of the third inverter circuit and with the terminal IN as the inlet of the circuit arrangement for bridging high voltages with a switching signal, the outlet of the seventh inverter circuit is connected with the inlet of the sixth inverter circuit and the outlet of the sixth inverter circuit is connected with the inlet of the second inverter circuit of the voltage transmitter. In this manner, the signal, originating from a low-signal, moves inverted to the inlet IN onto the capacitor C2.

On page 7, lines 15-23, please amend this paragraph as follows:

~~The~~ Another embodiment of ~~claim 5~~, in which the inverter circuit comprises two

complementary transistors connected in series, leads to inverter circuits with almost ideal performance. Both transistors are alternately the active element and the load element. In a resting state, the power consumption with use of MOSFETs is very minimal. These are only due to leakage currents. Power consumption occurs only during switching over and, therefore, proportionally to working frequency. This exists by the recharging of the load capacities and, in small part, by a cross flow.

On page 8, lines 1-6, please amend this paragraph as follows:

The capacities for signal transmission between the voltage transmitter and the voltage receiver are charged to the voltage differential to be overcome, ~~according to the embodiment of claim 6~~. For signal transmission, its value varies only to ΔQ , whereby the power consumption is independent from the voltage differential to be overcome.

On page 8, lines 8-16, please amend this paragraph as follows:

The circuit arrangement for bridging high voltages with a switching signal can be realized as integrated semi-conductor circuits made with semi-conductor processes, on the one hand, with CMOS circuits as the inverter circuits and, on the other hand, as a stack of layers with circuit stopper implantation, field oxide, poly-silicon, CVD-oxide, metal, CVD-oxide, metal, and so on, whereby the layers are electrically alternatingly connected, ~~according to claim 7~~. This fulfills advantageously the requirements for minimal power consumption and minimal space requirements.

On page 8, lines 18-20, please amend this paragraph as follows:

~~The~~ An embodiment of ~~claim 8~~, whereby the voltage transmitter, the capacitors, and the voltage receiver, respectively, are surrounded by trenches for voltage isolation, represents a favorable realization.

On page 8, line 22 through page 9, line 5, please amend this paragraph as follows:

An essential advantage of the circuit arrangement for bridging high voltages with a switching signal, as provided in claim 9, is that the semi-conductor processes for integrated high voltage circuits can be applied with any isolation for the voltage transmitter, the high voltage capacitors, and the voltage receiver. Therefore, the multifaceted variations for realizing the present invention are provided according to economic requirements, method technology manufacturing requirements, and/or supplied application specifications.

On page 9, line 6, please insert the following heading:

--Brief Description of the Drawings--

On page 10, line 4, please insert the following heading:

--Description of Specific Embodiments--.

On page 18, after line 20, please insert the following two new paragraphs:

--The specification incorporates by reference the disclosure of German priority document 102 46 083.3 filed September 27, 2002 and PCT/DE2003/003264 filed September 25, 2003.

The present invention is, of course, in no way restricted to the specific disclosure of the specification and drawings, but also encompasses any modifications within the scope of the appended claims.--

In addition, please add the attached abstract to the specification.